

FIG. 1 : PRIOR ART

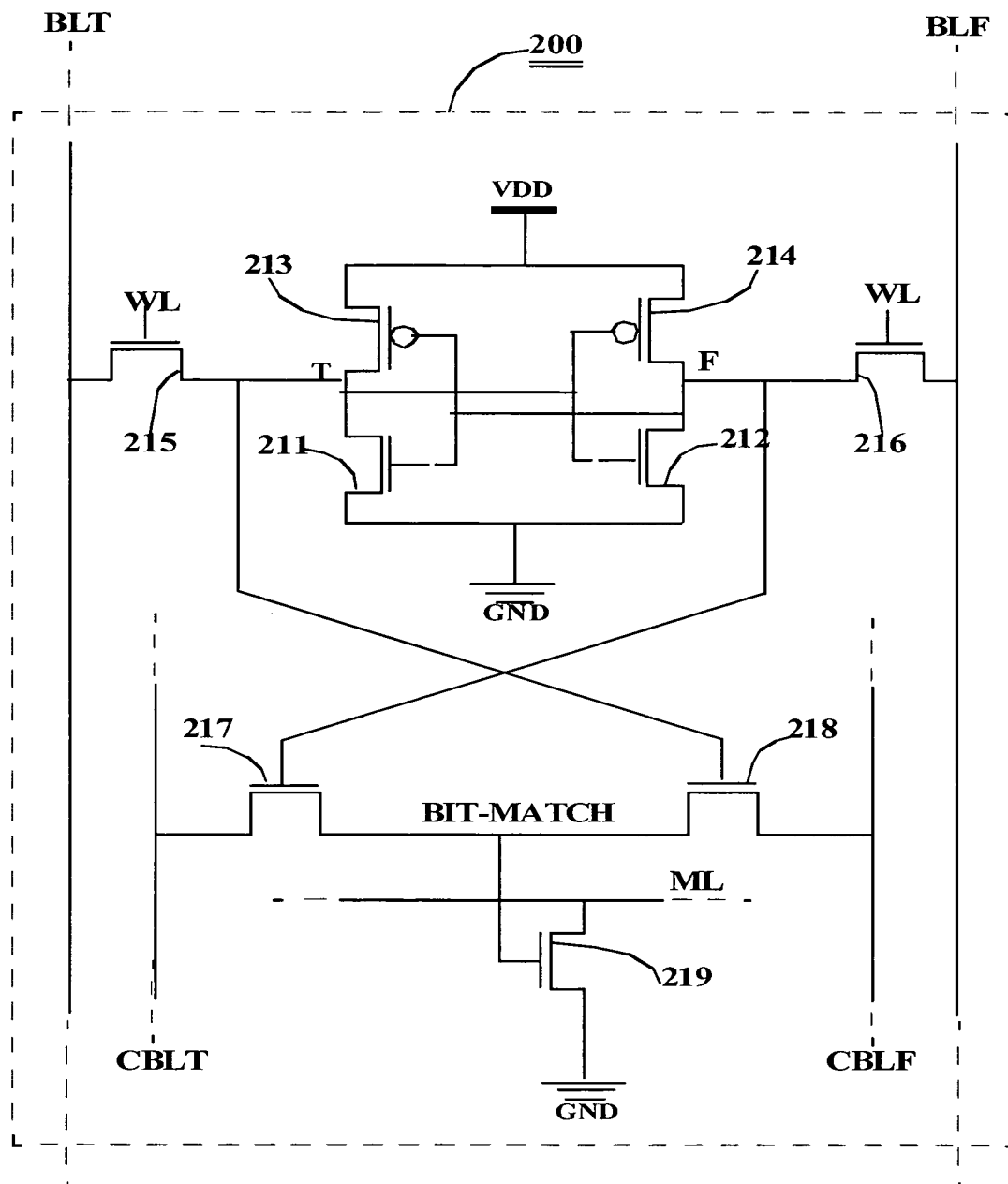


FIG. 2 : PRIOR ART

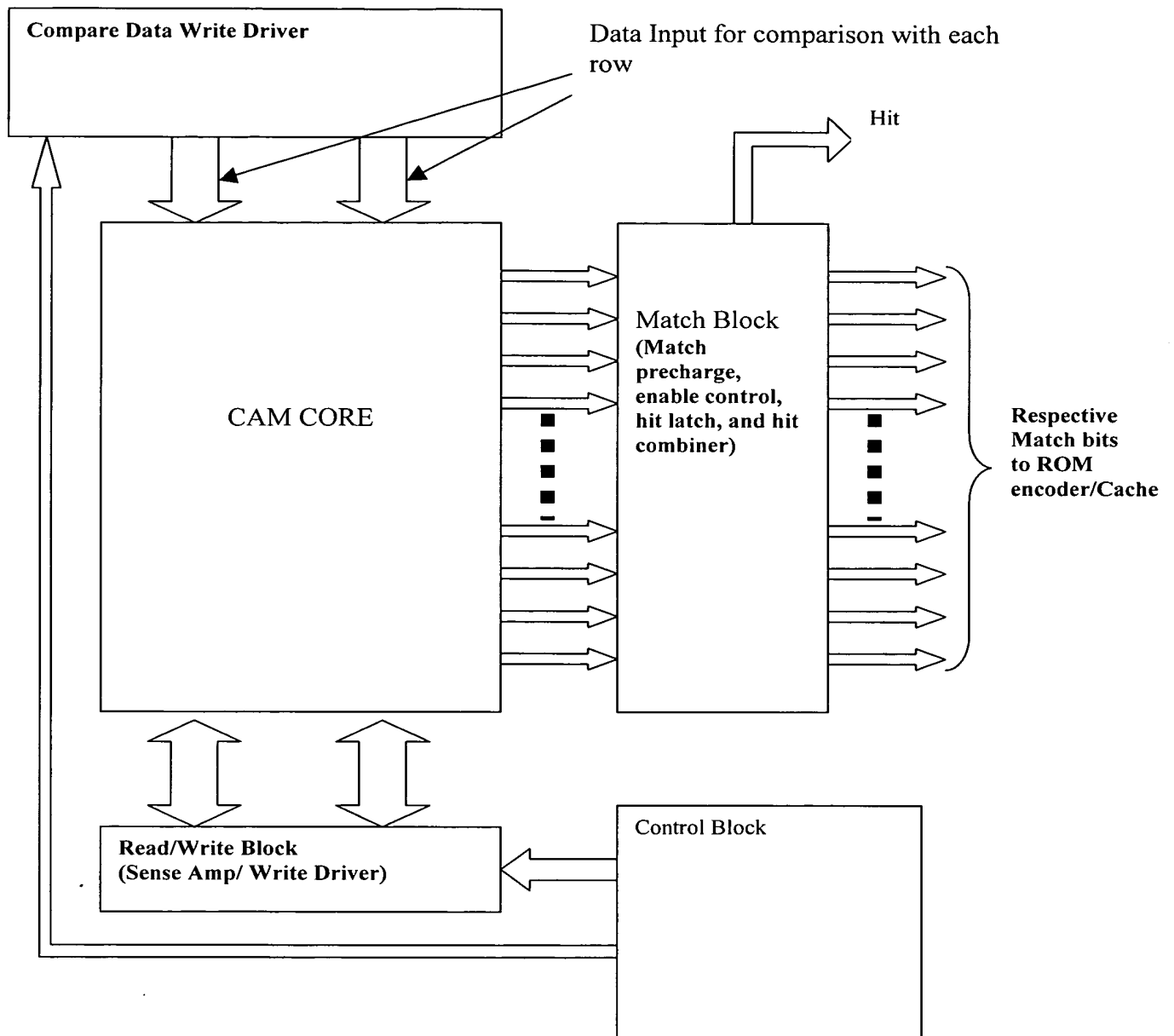


Figure No.3 : The full Architecture

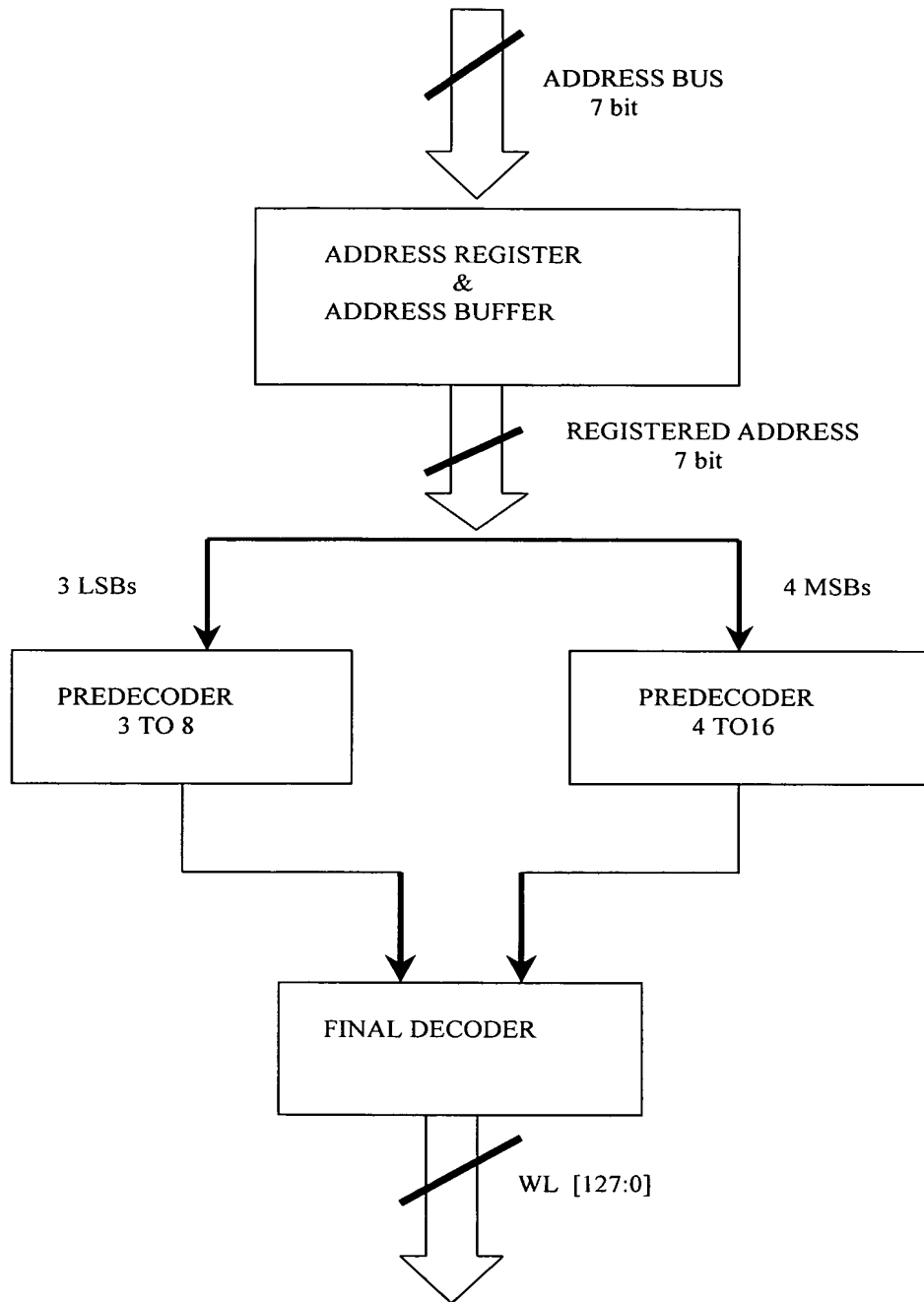


Figure 4: Decoder Block

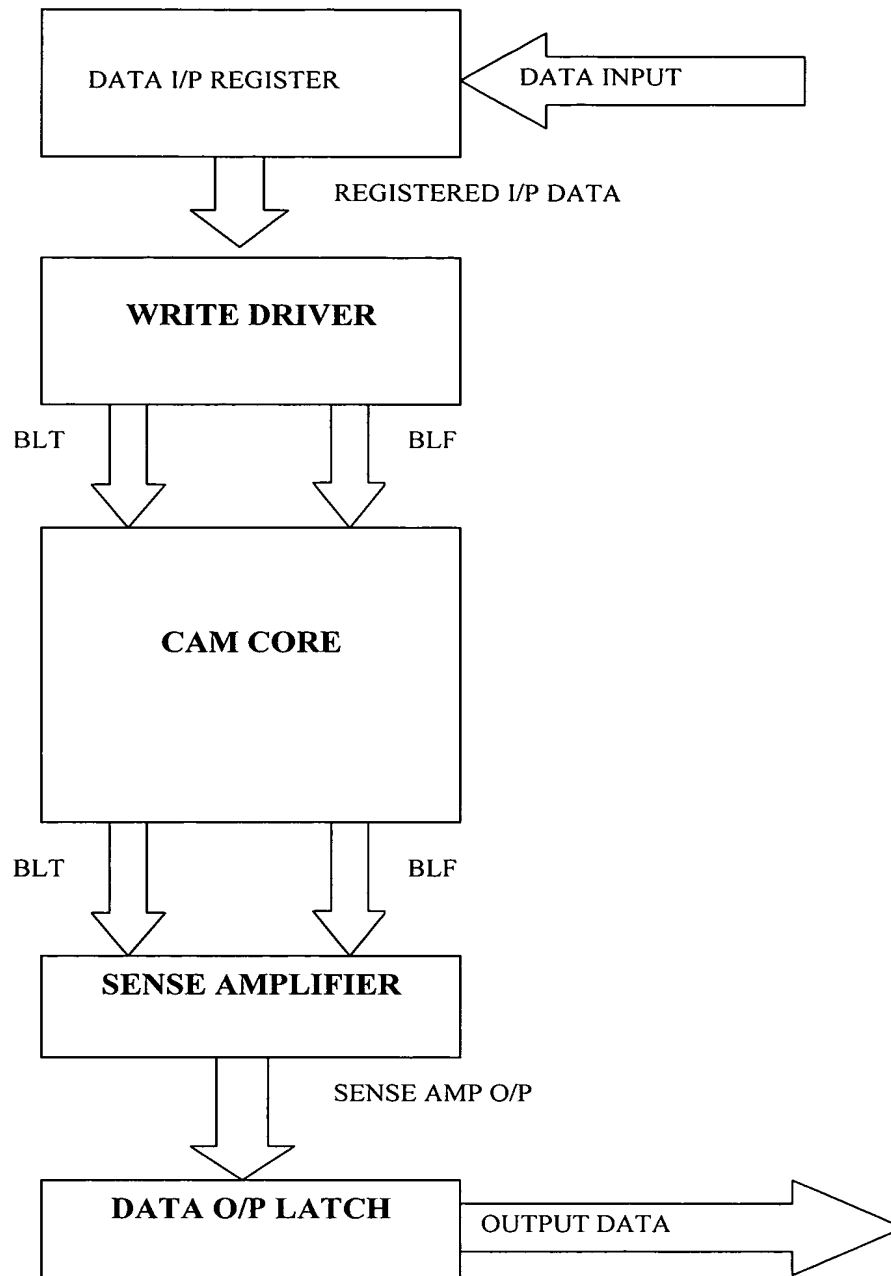


Figure No. 5 : Normal Read Write Operation in CAM

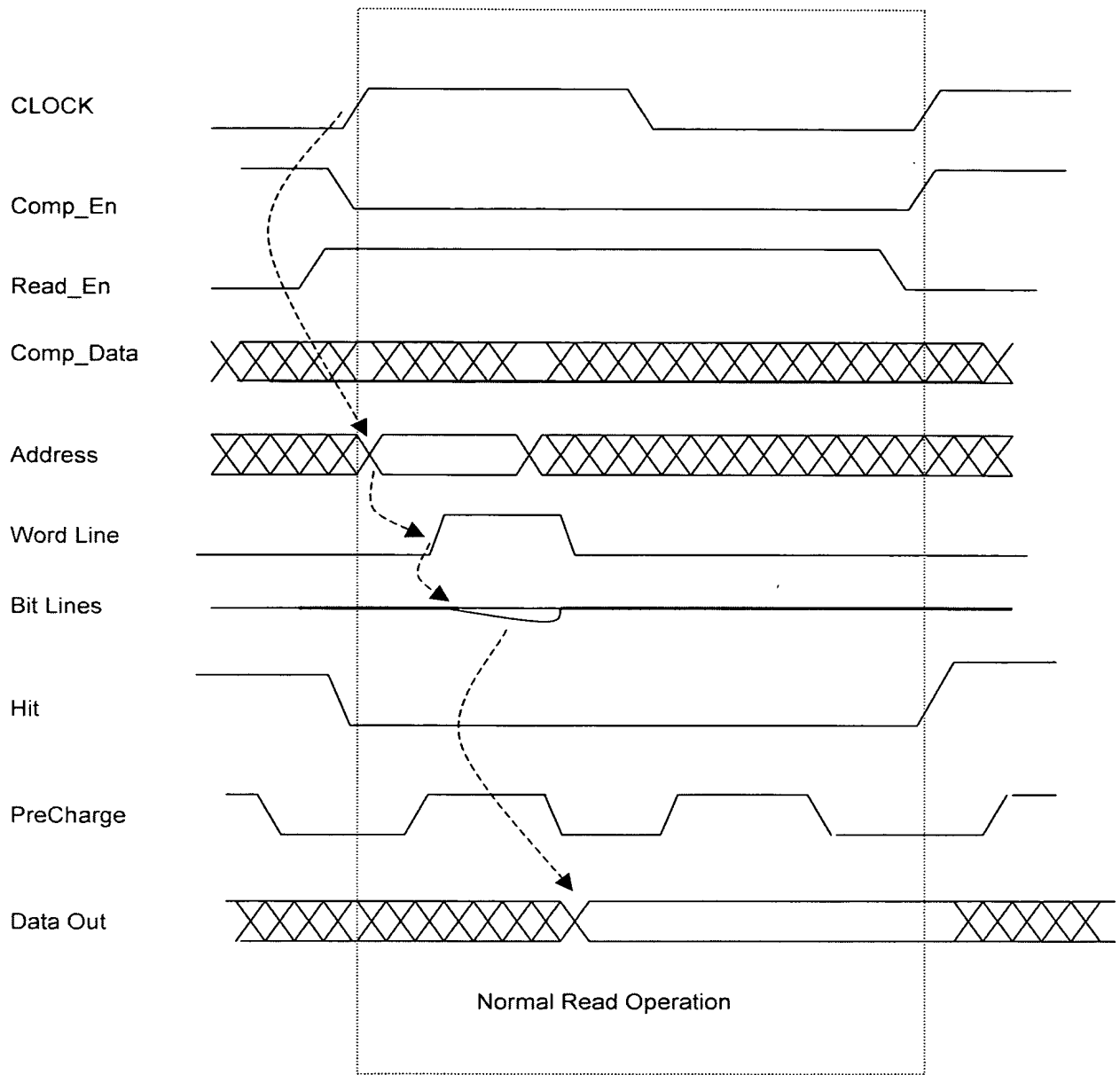


Figure 6 : Wave Form for Normal Read Operation

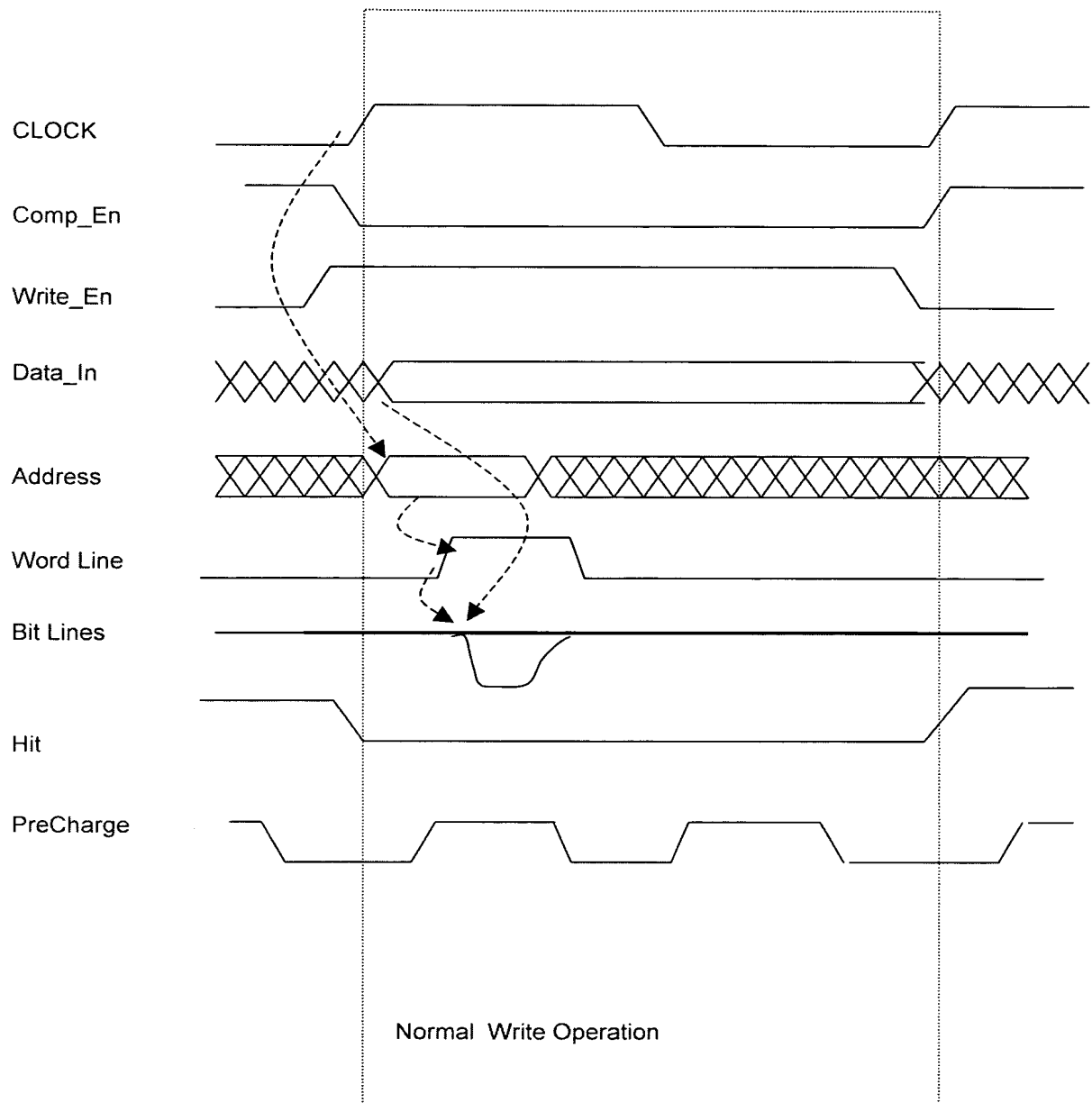


Figure7 Normal Write Operation

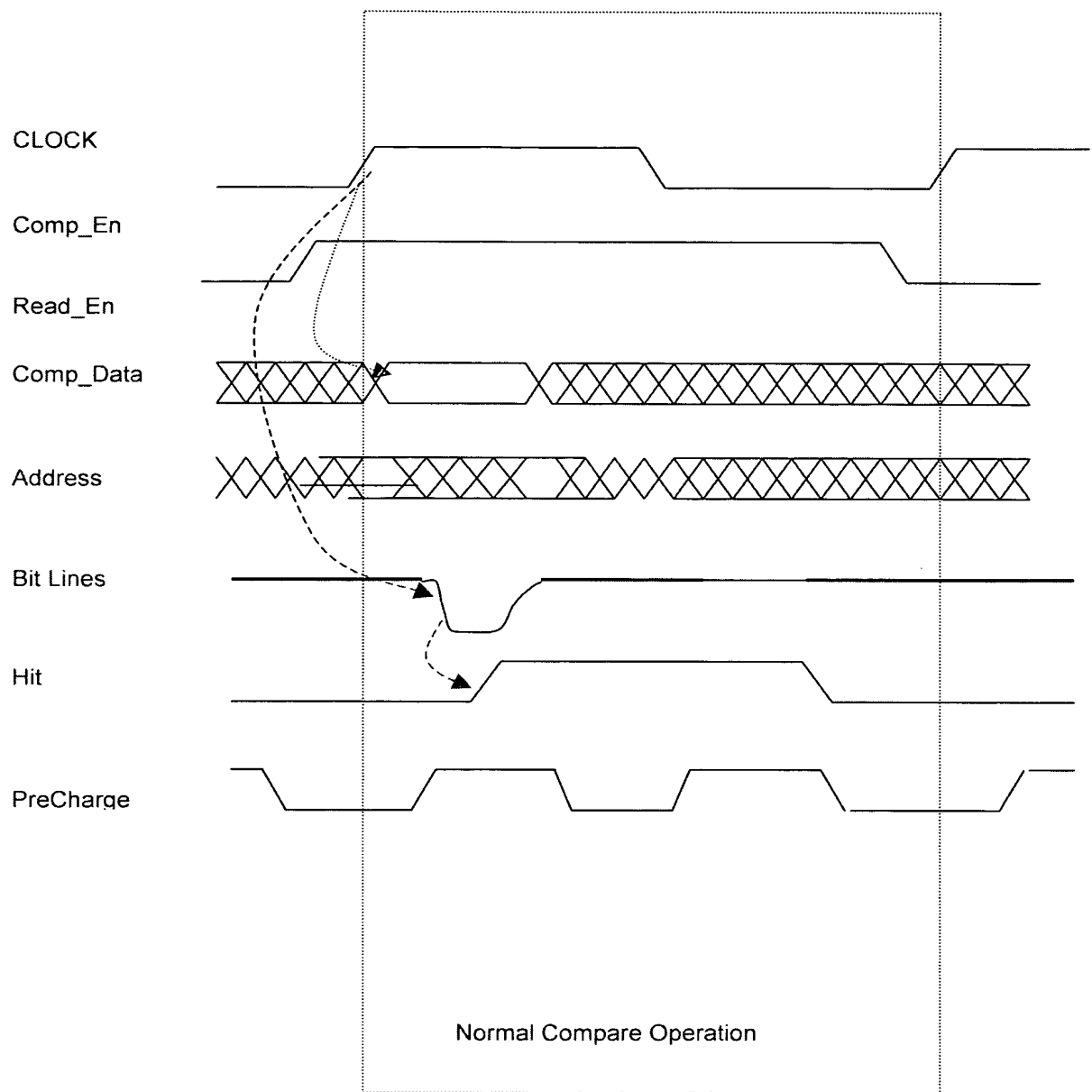


Figure 8 Normal Compare Operation

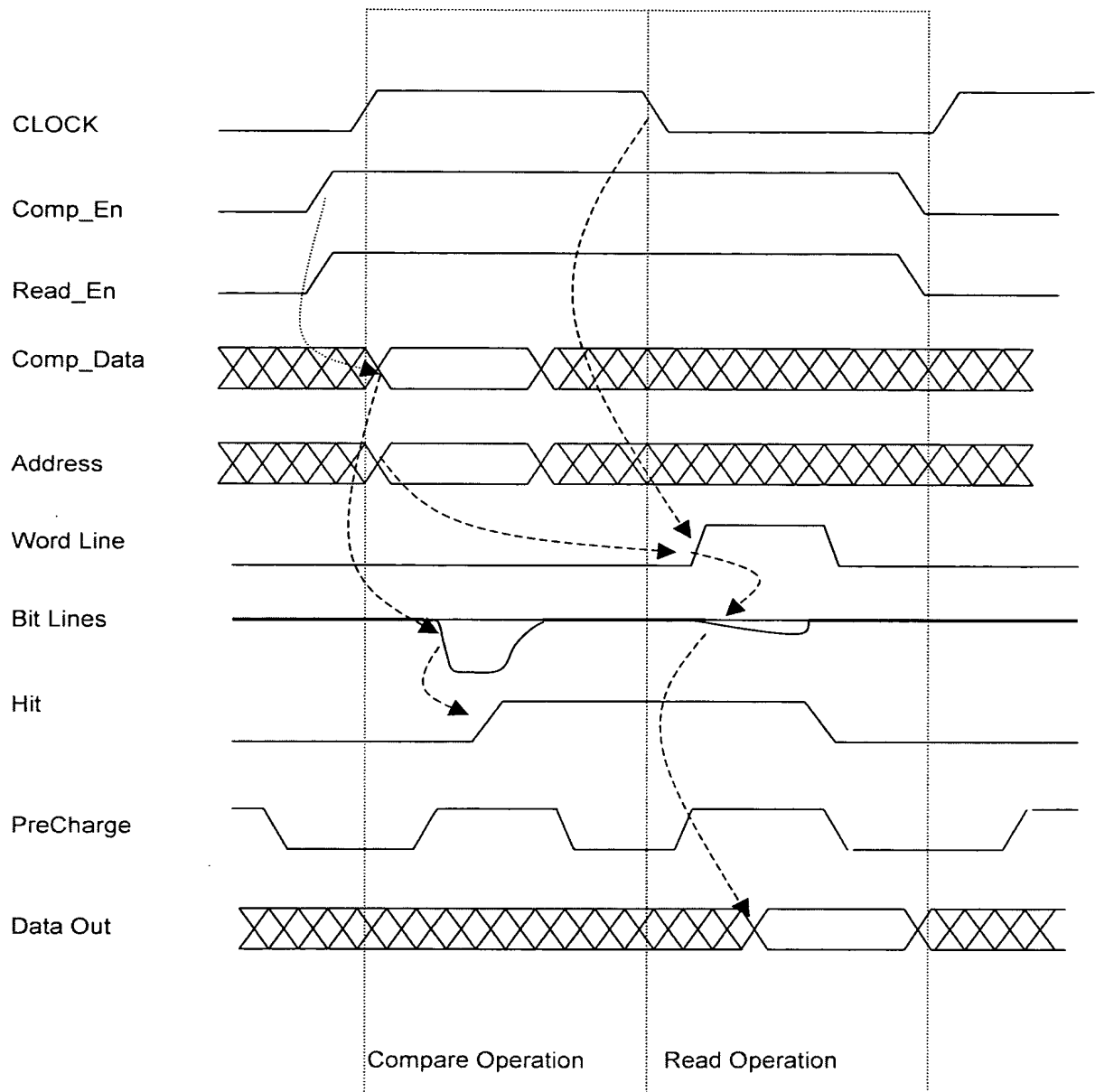


Figure 9 Compare & Read Operation in one Cycle

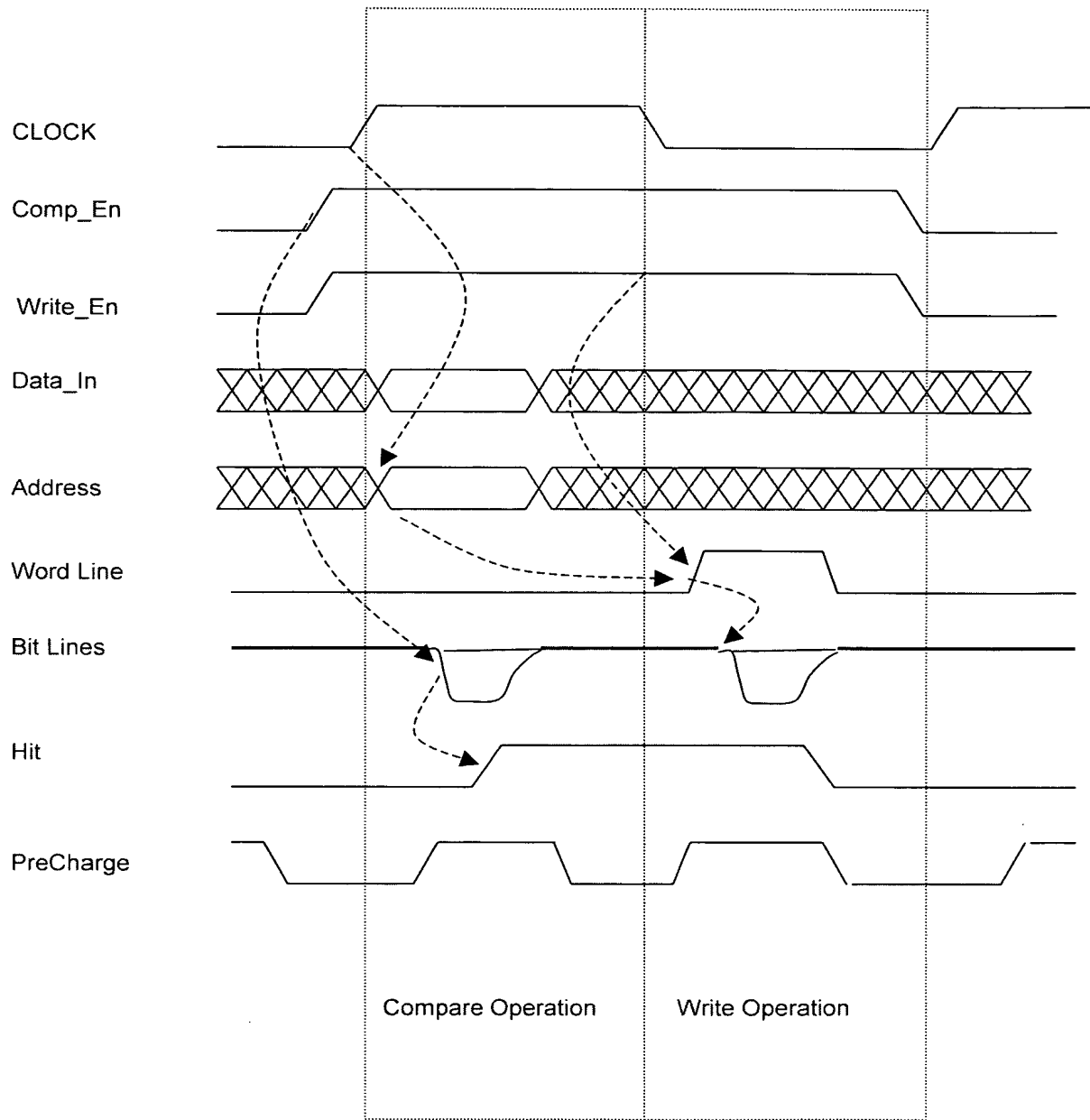


Figure 10 Compare & Write Operation in one Cycle